





logic code for determining an optimal trade-off between said context switching overhead and said optimal granularity.

Claim 12 (Original): The computer program product of claim 7, wherein said logic code for building includes:

- logic code for determining a size for a data cache based on said extracting;
- logic code for implementing a hierarchical caching structure in said data cache; and
- logic code for applying said data cache in said specific time-sliced architecture.

Claim 13 (Original): A time-sliced processor for use in a spread spectrum system comprising:

- a master control unit including a time slot table and a partial sums search table;
- a data cache for receiving input data; and
- a plurality of finger processing elements, each element comprising:
  - a cache for receiving data from the data cache,
  - a data selector connected to an output of the cache,
  - a despreader connected to an output of the data selector, and
  - a symbol integrator connected to an output of the despreader.